Remarks/Arguments

Claims 4-10, 13, and 18-20 were previously cancelled. In this response, claims 3 and 12 have been cancelled while claims 1, 2, 11, 14-16, and 21 have been amended.

Rejections under 35 U.S.C. § 112

Claims 14-16 were rejected under 35 U.S.C. § 112, second paragraph, for being dependent upon a previously cancelled base claim, claim 13. Accordingly, claims 14-16 have been amended. In light of these amendments, reconsideration of this rejection is respectfully requested.

Rejections under 35 U.S.C. § 102(b)

In the Office Action, claims 1 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,675,160 to Ryuichi Oikawa (herein "*Oikawa*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

As for claim 1, claim 1 has been amended and currently recites:

> A two-transistor DRAM cell consisting:
> an NMOS device with a first gate adapted to couple with write word line, a first controlled node adapted to couple with write bit line, and a second controlled node;
> a PMOS device with a second gate, a third controlled node adapted to couple with a read word line, and a fourth controlled node adapted to couple with read bit line, the second gate of the PMOS device coupled to the second controlled node of the NMOS device; and
> a storage node coupled to the second gate of the PMOS device and the second controlled node of the NMOS device, wherein the NMOS and PMOS devices are adapted to provide to the storage node a capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device.
>
> * Underline added.

In the Office Action, the Examiner alleged that in FIG. 4 of *Oikawa*, a two-transistor DRAM cell as recited in claim 1 is disclosed. Applicants respectfully disagree.

In particular, the two-transistor DRAM cell disclosed in *Oikawa* includes a capacitor, which is **not** recited in claim 1. Note that in claim 1, the word "consisting" (as opposed to comprising) is used. Therefore, *Oikawa* does not anticipate claim 1.

Further, note that the capacitor (CC) in FIG. 4 of *Oikawa* is coupled at one end to the storage node (n2) and coupled to the word line (WL) at the other end. Thus, the storage node as taught in *Oikawa* would not have a "capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device" as recited in amended claim 1. For at least these reasons, claim 1 is patentable over *Oikawa*. Claim 21 has similar features as claim 1, and therefore, is also patentable over *Oikawa*.

Claims 1-3, 11-12, and 21-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,314,017 to Emori et al. ("*Emori*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

Claim 1, as previously alluded to, has been amended and now includes, among other things, the features "wherein the NMOS and PMOS devices are adapted to provide to the storage node a capacitance equal to a sum of parasitic capacitances of the second controlled node of the NMOS device and the second gate of the PMOS device." Such features are not disclosed in *Emori*. That is, *Emori* **specifically** teaches a storage node with a capacitance equivalent only to the parasitic capacitance of the second gate (i.e., the gate and the drain of the read transistor Q2). See, for example, col. 9, lines 3-8, and Figures 1, 4, 12, and 16. For at least these reasons, claim 1 is patentable over *Emori*.

Amended independent claims 11 and 21 have similar features as claim 1, and therefore, are likewise patentable over *Emori*. Claims 2, 22, and 23 depend from claims 1, 11, and 21, respectively, incorporating their features. Therefore, claims 2, 22, and 23 are also patentable over *Emori*.

Conclusion

In view of the foregoing, the Applicants respectfully submit that claims 1-2, 11, 14-17 and 21-23 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at 503-796-2099.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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